a gate electrode located on the gate insulating layer in each of the plurality of trenches;

a source electrode electrically coupled with the source region and the base region;

a drain electrode located on the second surface of the substrate;

a deep layer located under the base region and extending to a depth deeper than the plurality of trenches, the deep layer having the second conductivity type, the deep payer having a plurality of stripe portions and an outer edge portion surrounding the plurality of stripe portions, the plurality of stripe portions arranged in a stripe pattern, each of the plurality of stripe portions formed in parallel with a planer direction of the substrate along a second direction crossing the first direction, the outer edge portion of the deep layer located at an outer edge portion of the cell section and formed toward the peripheral section; and

a peripheral high-voltage part located at the peripheral section, wherein

an inversion channel is provided at a surface portion of the base region located on the sidewall of the trench and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

13. The silicon carbide semiconductor device according to claim **12**, wherein

the deep layer is formed at a whole area of the outer edge portion of the cell section.

14. The silicon carbide semiconductor device according to claim **12**, wherein:

the outer edge portion of the deep layer is at a first distance from the peripheral section;

the plurality of stripe portions of the deep layer is arranged at intervals of a second distance; and

the first distance is less than the second distance.

15. The silicon carbide semiconductor device according to claim **12**, wherein:

the outer edge portion of the deep layer has an opening; and

the opening is filled with a depletion layer expanding from the deep layer when the voltage is not applied to the gate electrode.

16. The silicon carbide semiconductor device according to claim **12**, wherein:

the peripheral high-voltage part includes a mesa structure portion and a reduced surface field (RESURF) layer;

the mesa structure portion has a recess part deeper than the base region; and

the RESURF layer extends from a bottom surface of the recess part to a predetermined depth and surrounds the cell section.

17. The silicon carbide semiconductor device according to claim **16**, wherein:

the deep layer is formed at the whole area of the outer edge portion of the cell section; and

the deep layer is connected with the RESURF layer.

18. The silicon carbide semiconductor device according to claim **16**, wherein:

the outer edge portion of the deep layer is at a first distance from the RESURF layer;

the plurality of stripe portions of the deep layer is arranged at intervals of a second distance; and

the first distance is less than the second distance.

19. A silicon carbide semiconductor device comprising:

a substrate made of silicon carbide, the substrate having one of a first conductivity type and a second conductivity type, the substrate having first and second opposing surfaces;

a drift layer located on the first surface of the substrate, the drift layer made of silicon carbide, the drift layer having the first conductivity type and having an impurity concentration less than an impurity concentration of the substrate, the drift layer having a cell section and a peripheral section surrounding the cell section;

a base region located on the cell section of the drift layer, the base region made of silicon carbide and having the second conductivity type;

a source region located on the base region, the source region made of silicon carbide, the source region having the first conductive type and having an impurity concentration greater than the impurity concentration of the drift layer;

a plurality of trenches extending to a depth deeper than the source region and the base region and reaching the drift layer, the plurality of trenches arranged in a stripe pattern, each of the plurality of trenches sandwiched by each of the base region and the source region, each of the plurality of trenches provided along a first direction;

a channel layer located on a surface of each of the plurality of trenches, the channel layer made of silicon carbide, the channel layer having the first conductivity type and having an impurity concentration less than the impurity concentration of the source region;

a gate insulating layer located on a surface of the channel layer in each of the plurality of trenches;

a gate electrode located on the gate insulating layer in each of the plurality of trenches;

a source electrode electrically coupled with the source region and the base region;

a drain electrode located on the second surface of the substrate;

a deep layer located under the base region and extending to a depth deeper than the plurality of trenches, the deep layer having the second conductivity type, the deep payer having a plurality of stripe portions and an outer edge portion surrounding the plurality of stripe portions, the plurality of stripe portions arranged in a stripe pattern, each of the plurality of stripe portions formed in parallel with a planer direction of the substrate along a second direction crossing the first direction, the outer edge portion of the deep layer located at an outer edge portion of the cell section and formed toward the peripheral section; and

a peripheral high-voltage part located at the peripheral section, wherein

an accumulation channel is provided at the channel layer and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

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